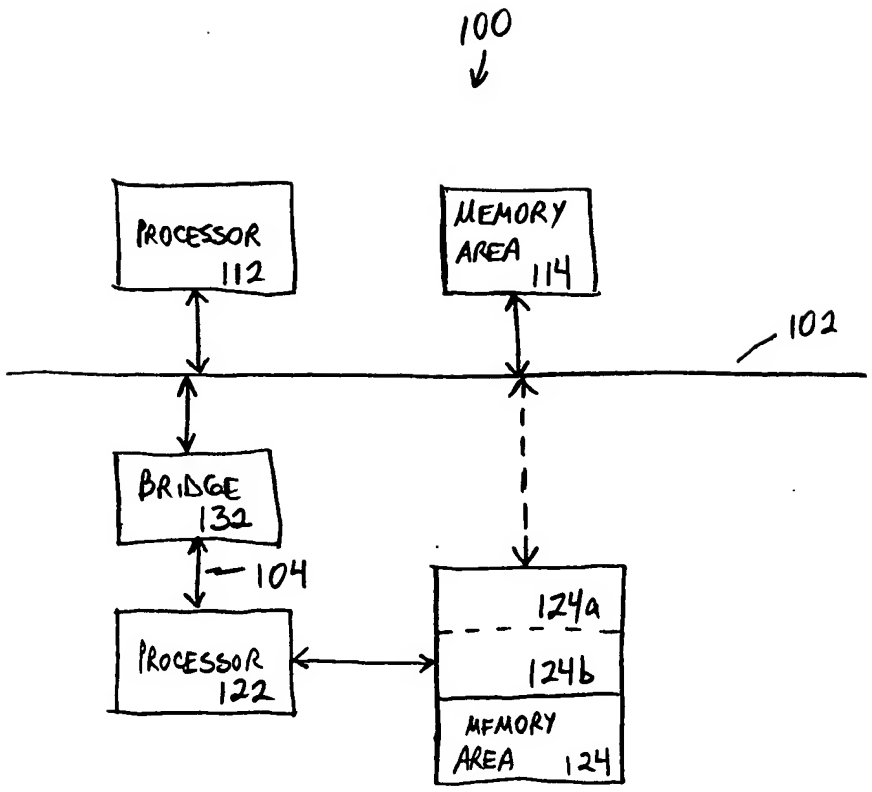
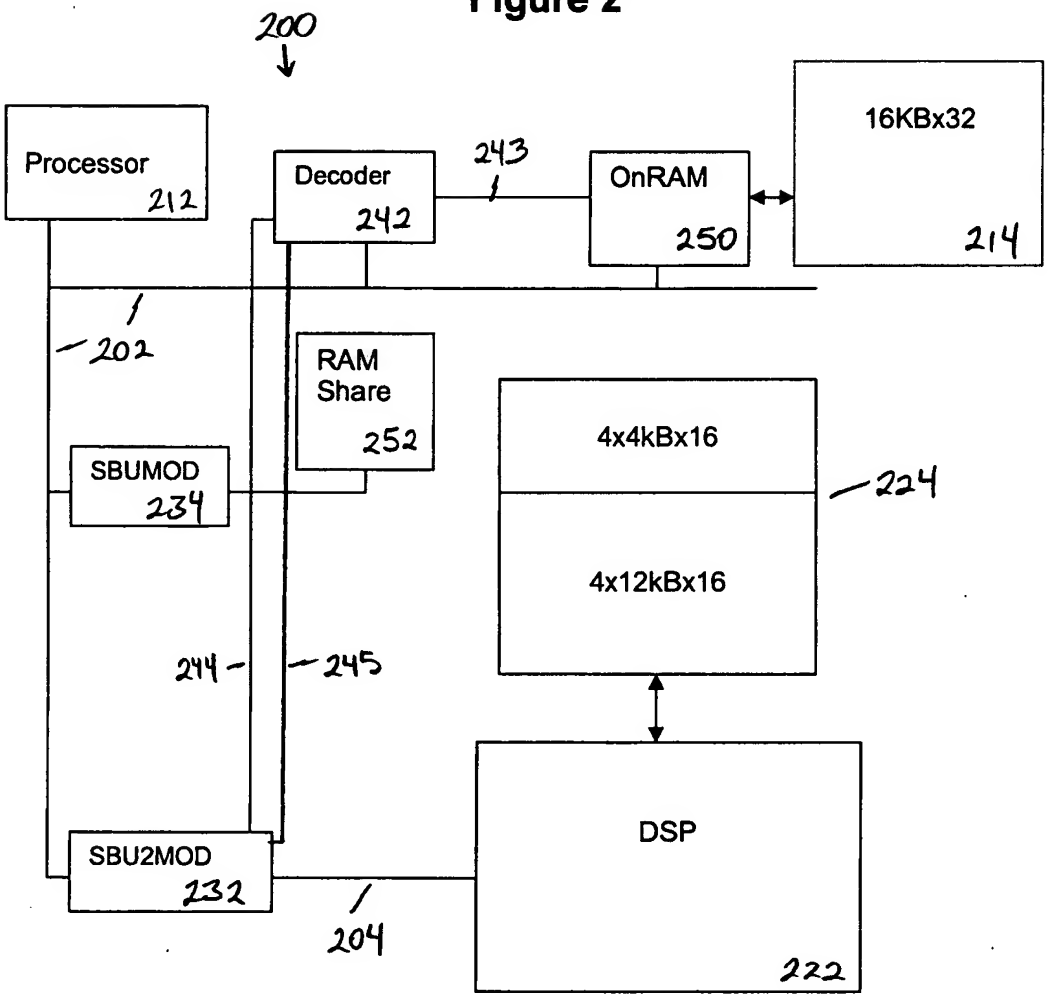

100
PROCESSOR
112
MEMORY
AREA
114
102
BRIDGE
132
104
PROCESSOR
122
124a
124b
MEMORY
AREA
124

FIGURE 1

Figure 2


200
Processor
212
Decoder
242
243
OnRAM
250
16KBx32
214
202
RAM
Share
252
SBUMOD
234
4x4kBx16
4x12kBx16
224
244
245
SBU2MOD
232
204
DSP
222

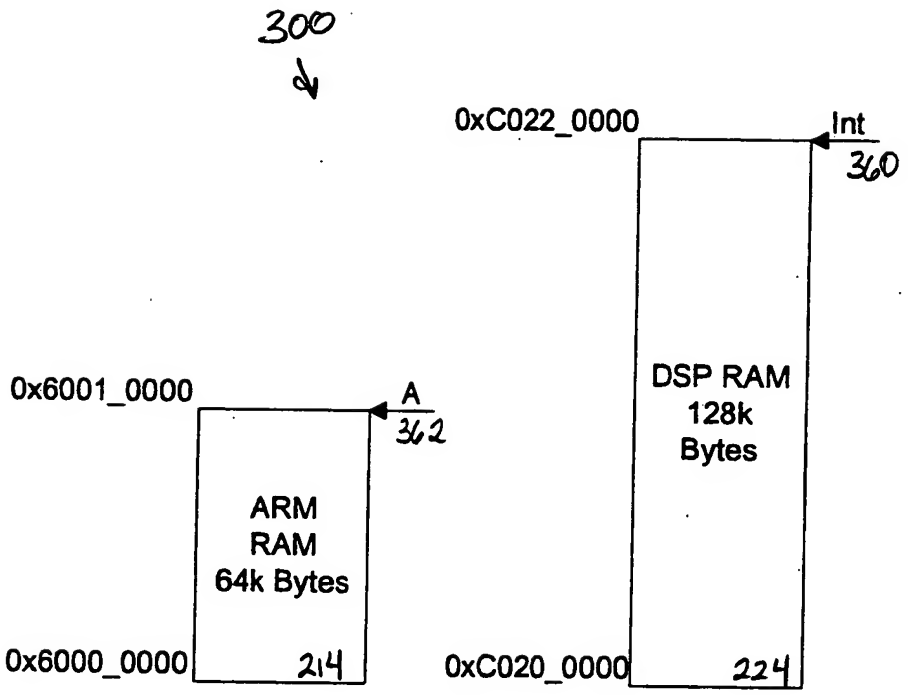
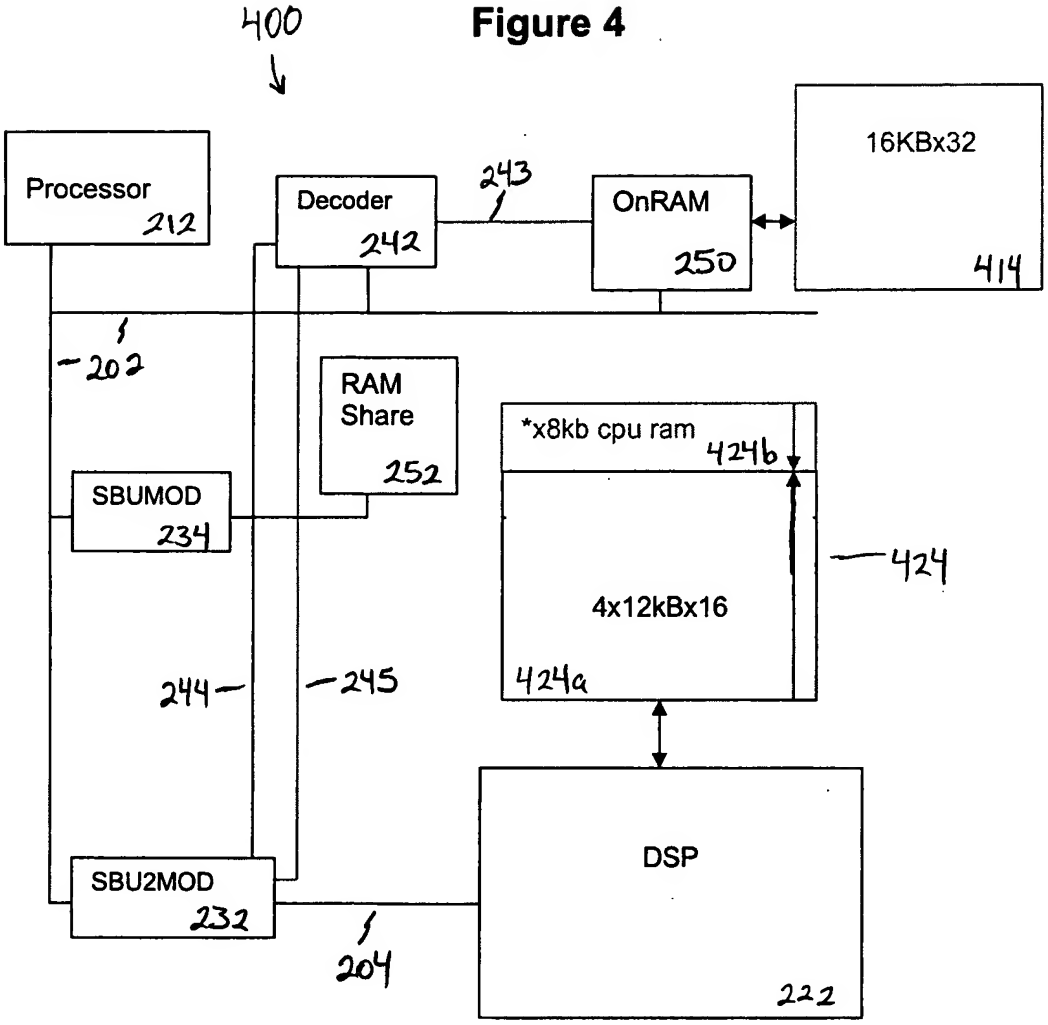

300
0xC022_0000
Int
360
0x6001_0000
A
362
ARM
RAM
64k Bytes
0x6000_0000
214
DSP RAM
128k
Bytes
0xC020_0000
224

FIGURE 3

Figure 4


400
Processor
212
Decoder
242
243
OnRAM
250
16KBx32
414
202
RAM
Share
252
*x8kb cpu ram
424b
SBUMOD
234
424
4x12kBx16
424a
244
245
DSP
222
SBU2MOD
232
204

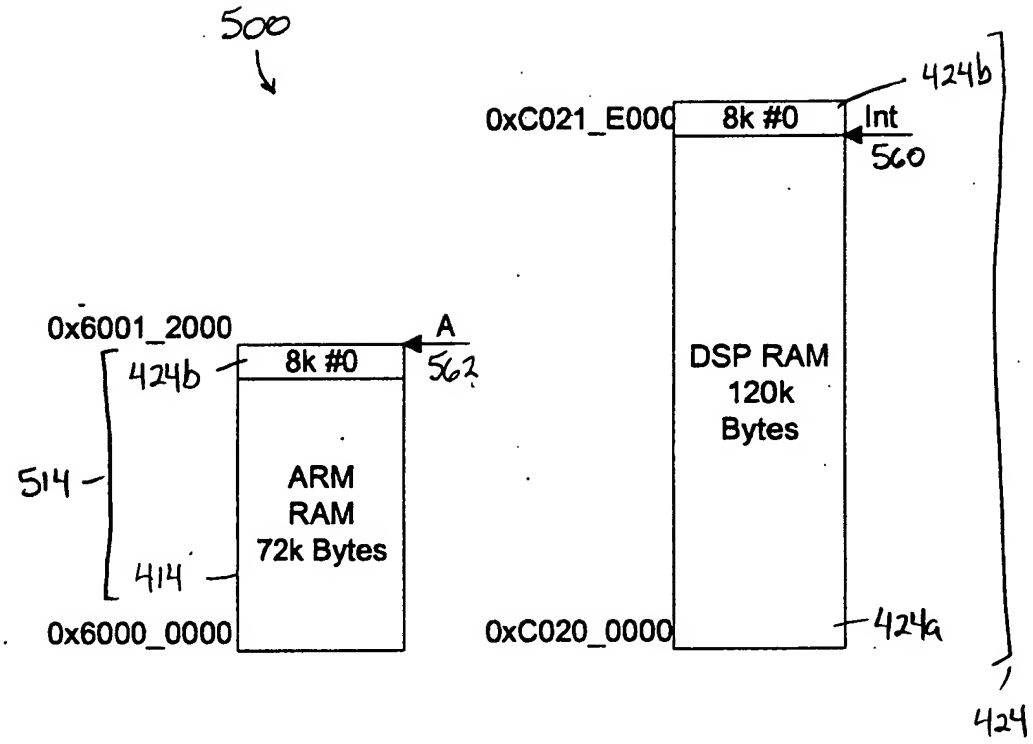

500
0xC021_E000
8k #0
Int
560
424b
DSP RAM
120k
Bytes
0xC020_0000
424a
424
0x6001_2000
A
562
424b
8k #0
514
ARM
RAM
72k Bytes
414
0x6000_0000

FIGURE 5A

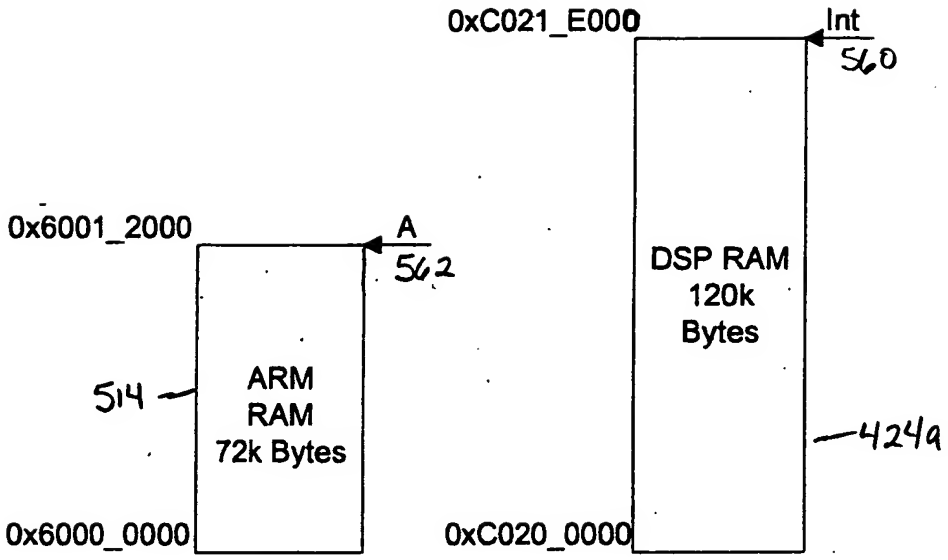

0xC021_E000
Int
560
0x6001_2000
A
562
514
ARM
RAM
72k Bytes
0x6000_0000
DSP RAM
120k
Bytes
424a
0xC020_0000

FIGURE 5B

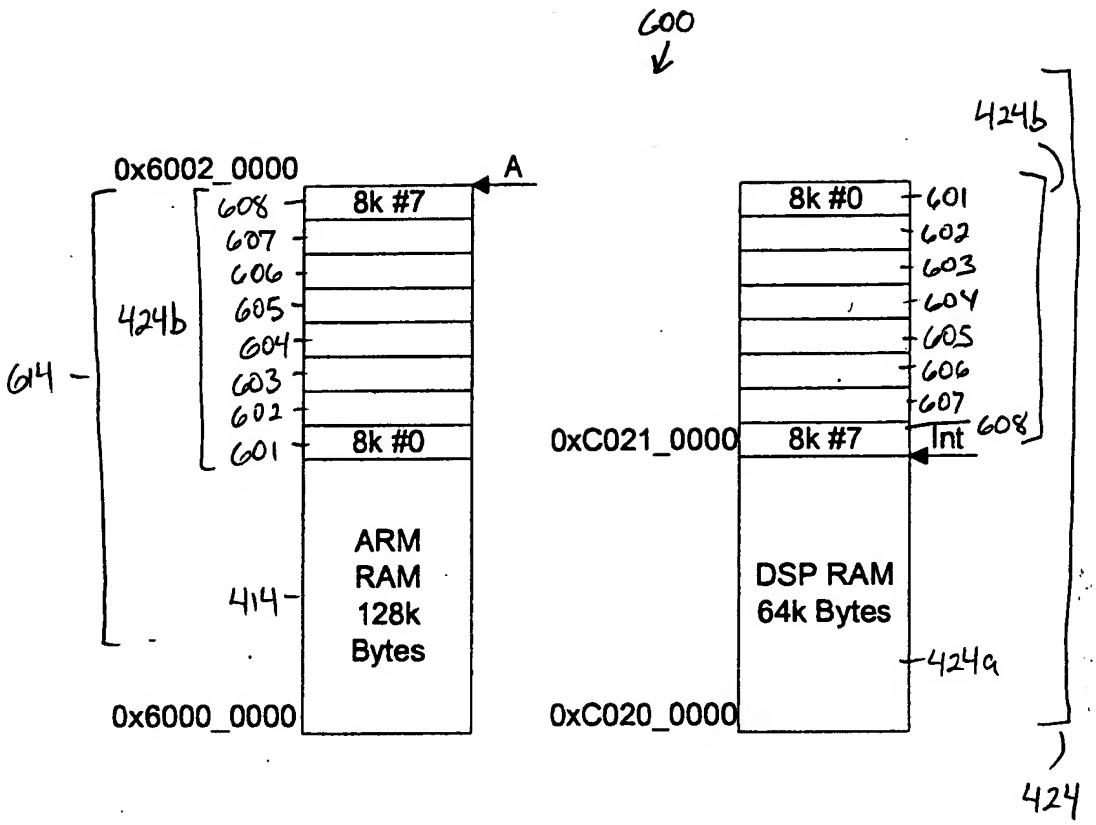

600
424b
0x6002_0000
A
608
607
606
605
604
603
602
601
8k #7
8k #0
424b
614
ARM
RAM
128k
Bytes
414
0x6000_0000
8k #0
601
602
603
604
605
606
607
0xC021_0000
8k #7
Int
608
DSP RAM
64k Bytes
424a
0xC020_0000
424

FIGURE 6A

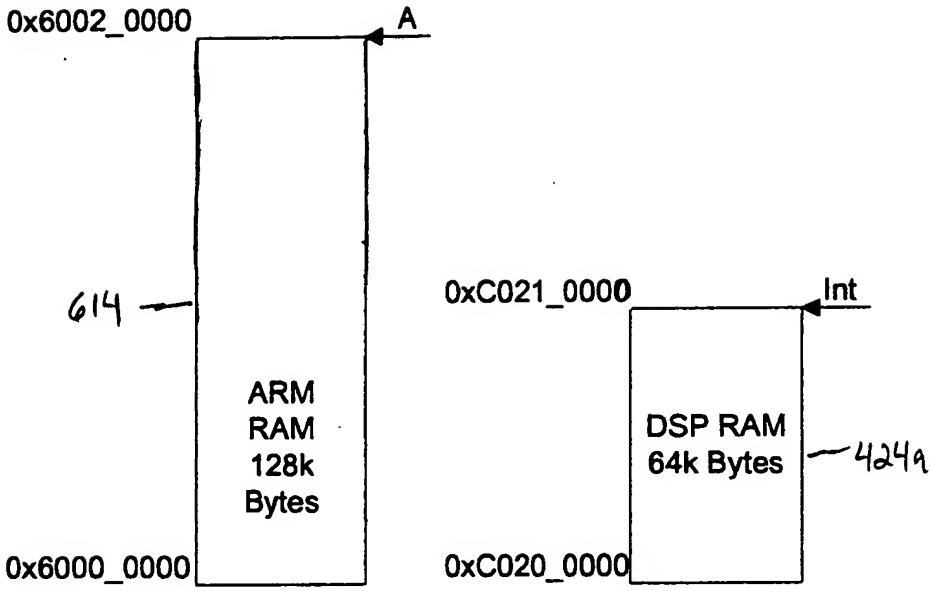
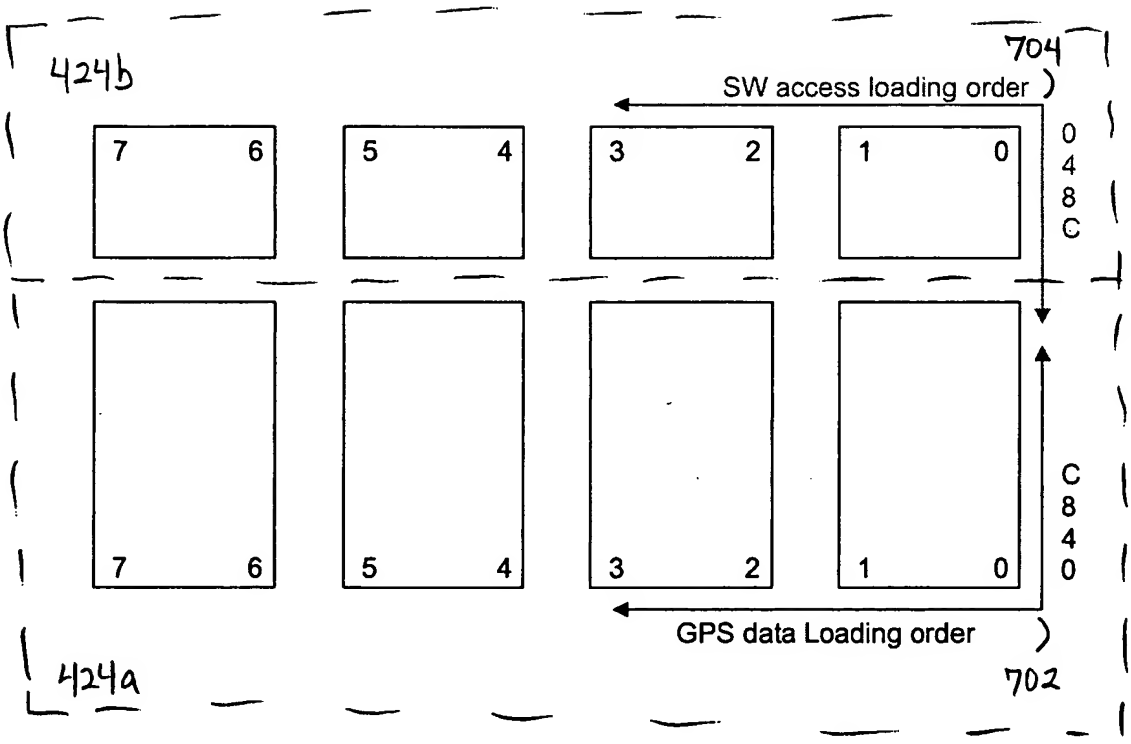
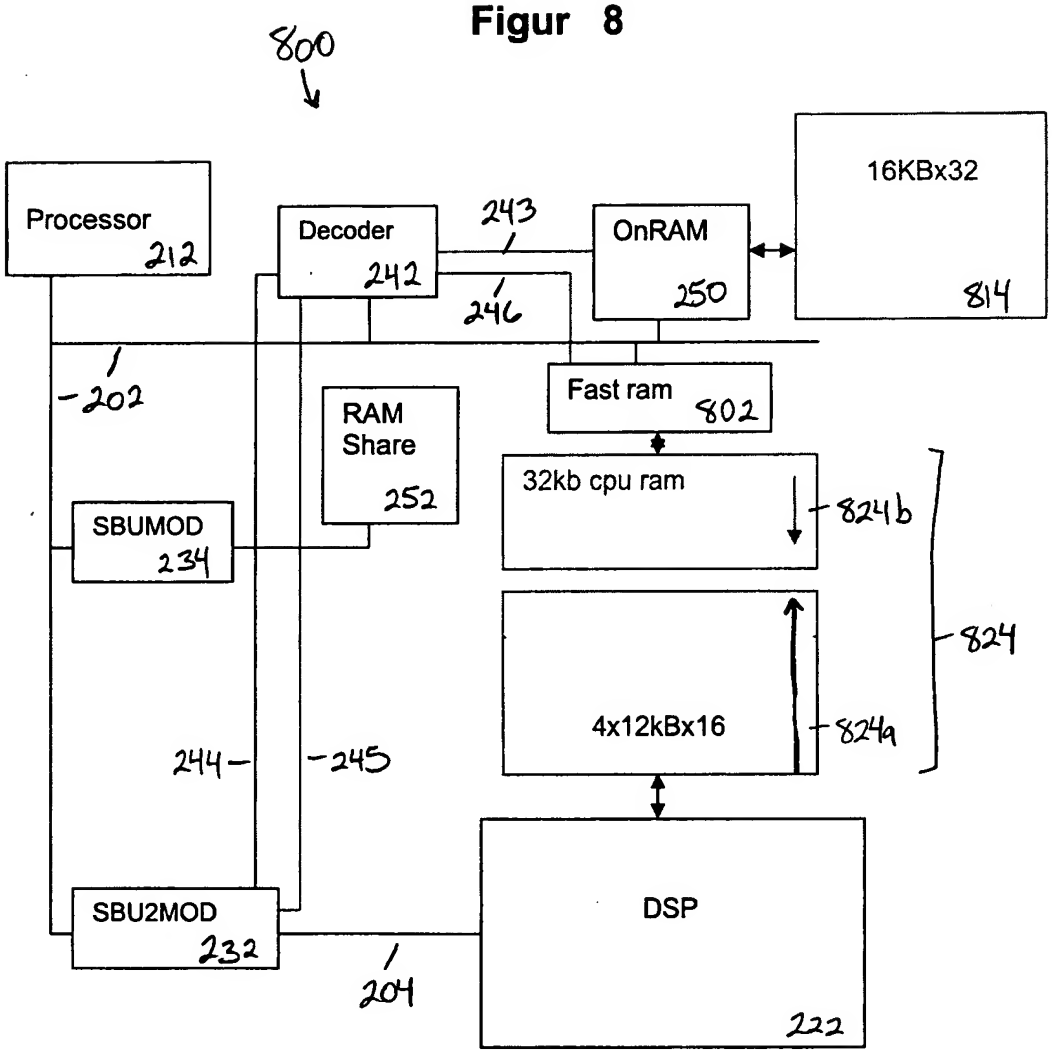

0x6002_0000
A
614
ARM
RAM
128k
Bytes
0x6000_0000
0xC021_0000
Int
DSP RAM
64k Bytes
424a
0xC020_0000

FIGURE 6B

Figur 7


424b
704
SW access loading order
7 6
5 4
3 2
1 0
0 4 8 C
C 8 4 0
7 6
5 4
3 2
1 0
GPS data Loading order
424a
702

Figur 8


800
Processor
212
Decoder
242
243
246
OnRAM
250
16KBx32
814
202
RAM
Share
252
Fast ram
802
32kb cpu ram
824b
824
4x12kBx16
824a
SBUMOD
234
244
245
SBU2MOD
232
204
DSP
222

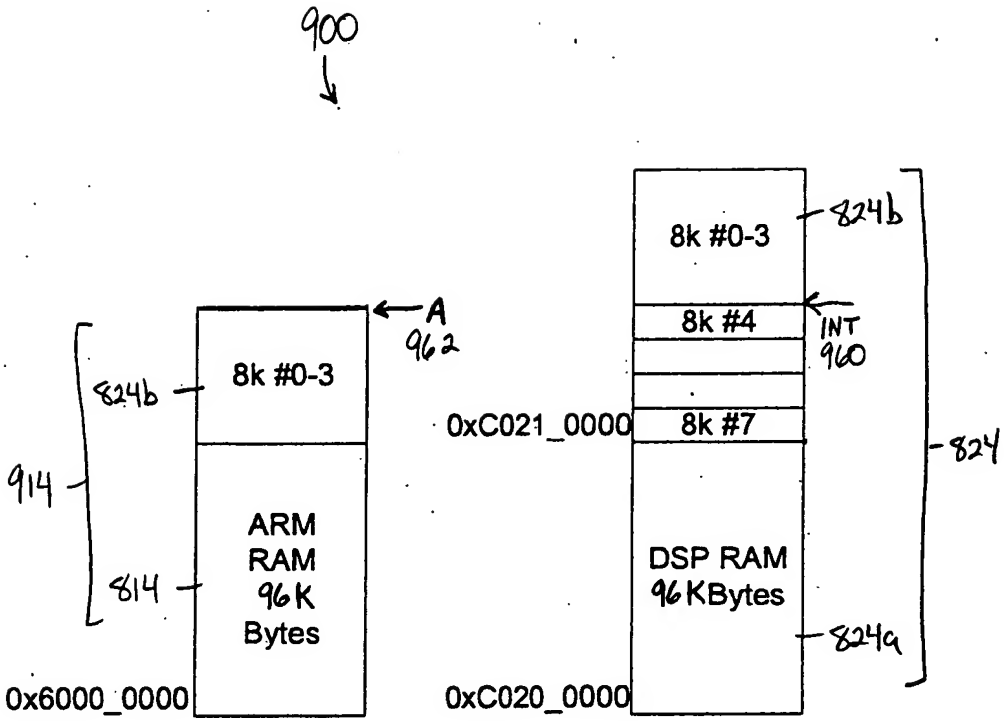

900
8k #0-3
824b
A
962
8k #4
INT
960
824b
914
0xC021_0000
8k #7
824
ARM
RAM
96K
Bytes
814
DSP RAM
96 KBytes
824a
0x6000_0000
0xC020_0000

FIGURE 9A

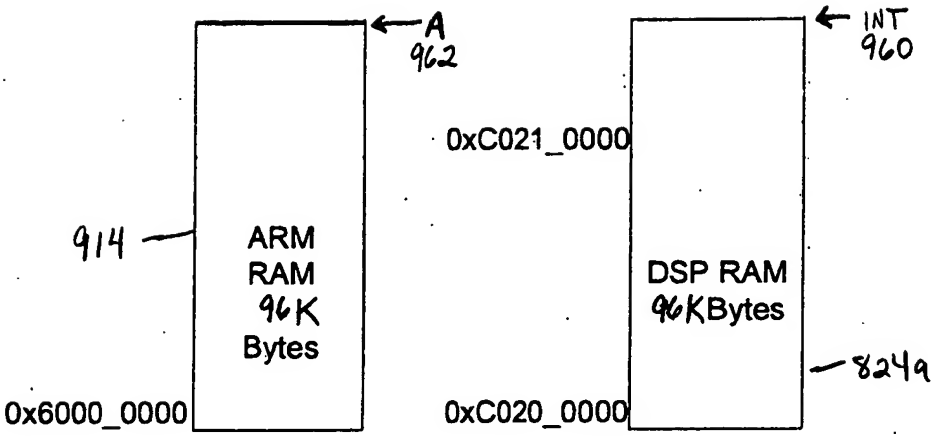
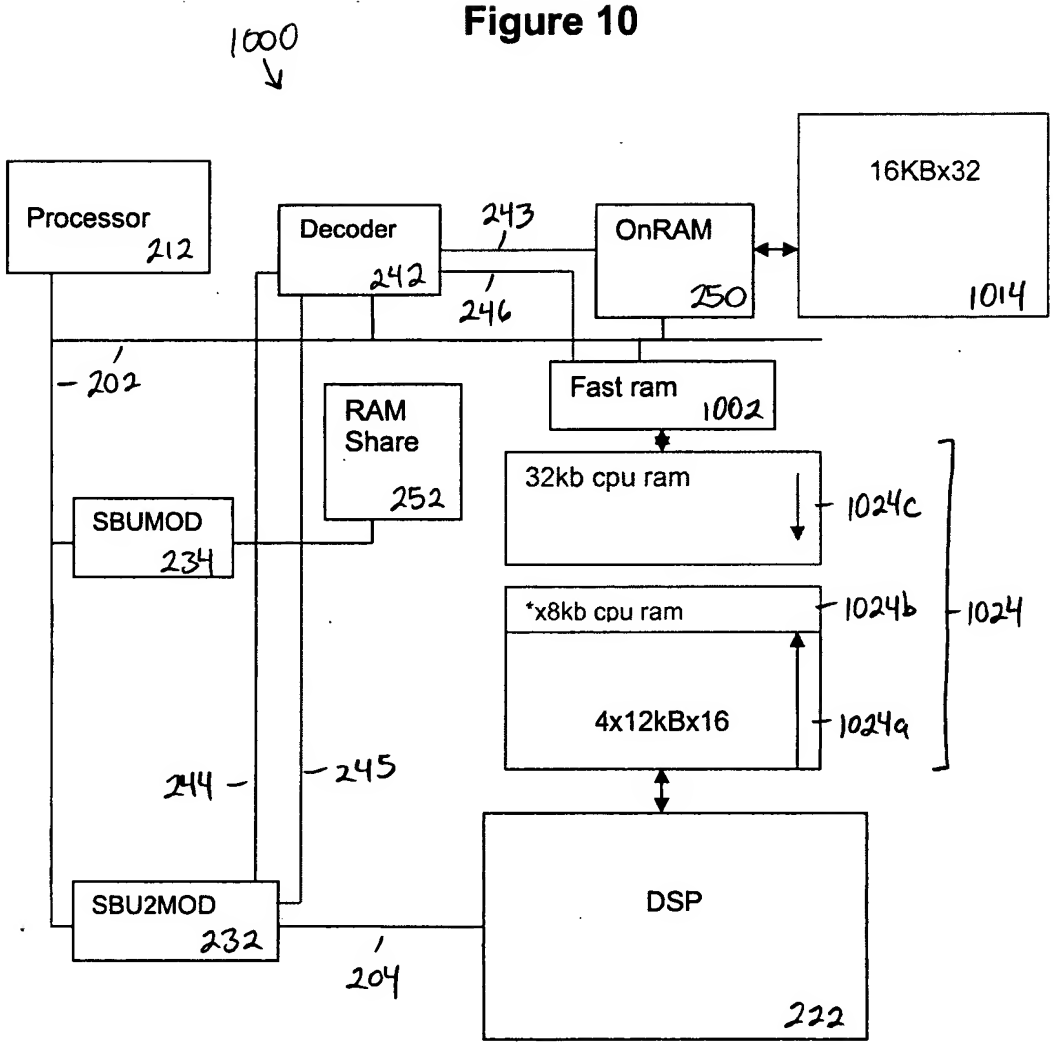

A
962
INT
960
0xC021_0000
914
ARM
RAM
96K
Bytes
DSP RAM
96KBytes
824a
0x6000_0000
0xC020_0000

FIGURE 9B

Figure 10


1000
Processor
212
Decoder
242
243
246
OnRAM
250
16KBx32
1014
202
RAM
Share
252
Fast ram
1002
32kb cpu ram
1024c
SBUMOD
234
*x8kb cpu ram
1024b
1024
4x12kBx16
1024a
244
245
SBU2MOD
232
204
DSP
222

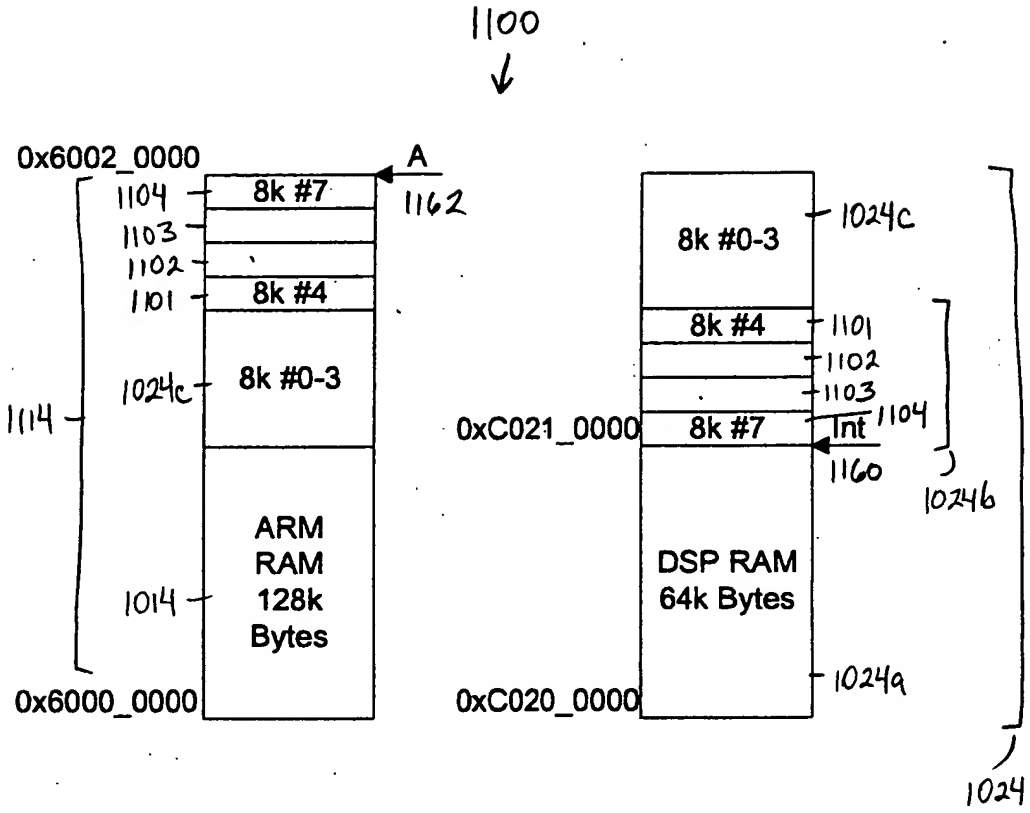

1100
0x6002_0000
A
1162
1104
8k #7
1103
1102
1101
8k #4
1024c
8k #0-3
1114
ARM
RAM
128k
Bytes
1014
0x6000_0000
8k #0-3
1024c
8k #4
1101
1102
1103
0xC021_0000
8k #7
Int
1104
1160
1024b
DSP RAM
64k Bytes
0xC020_0000
1024a
1024

FIGURE 11A

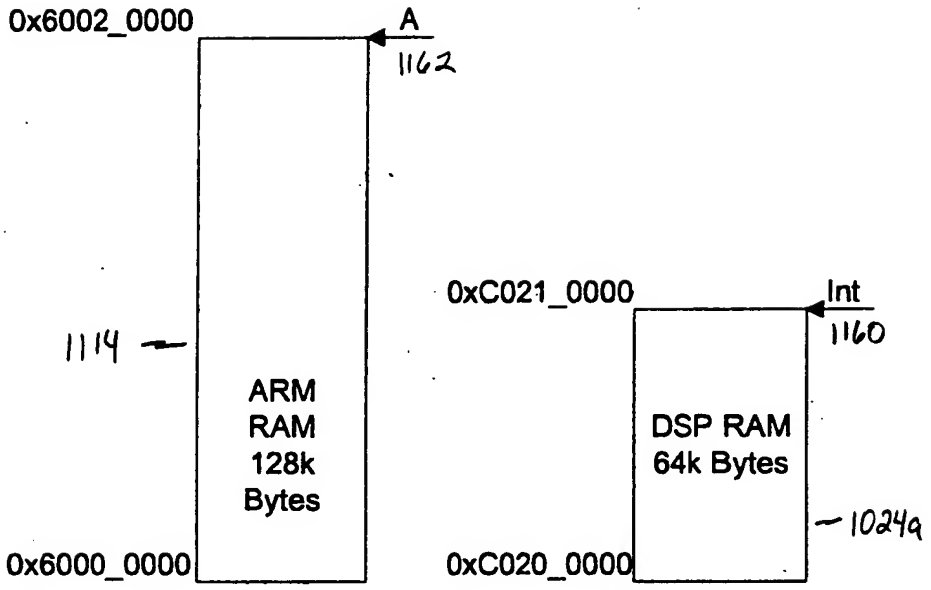

0x6002_0000
A
1162
1114
ARM
RAM
128k
Bytes
0x6000_0000
0xC021_0000
Int
1160
DSP RAM
64k Bytes
1024a
0xC020_0000

FIGURE 11B

Figur 12

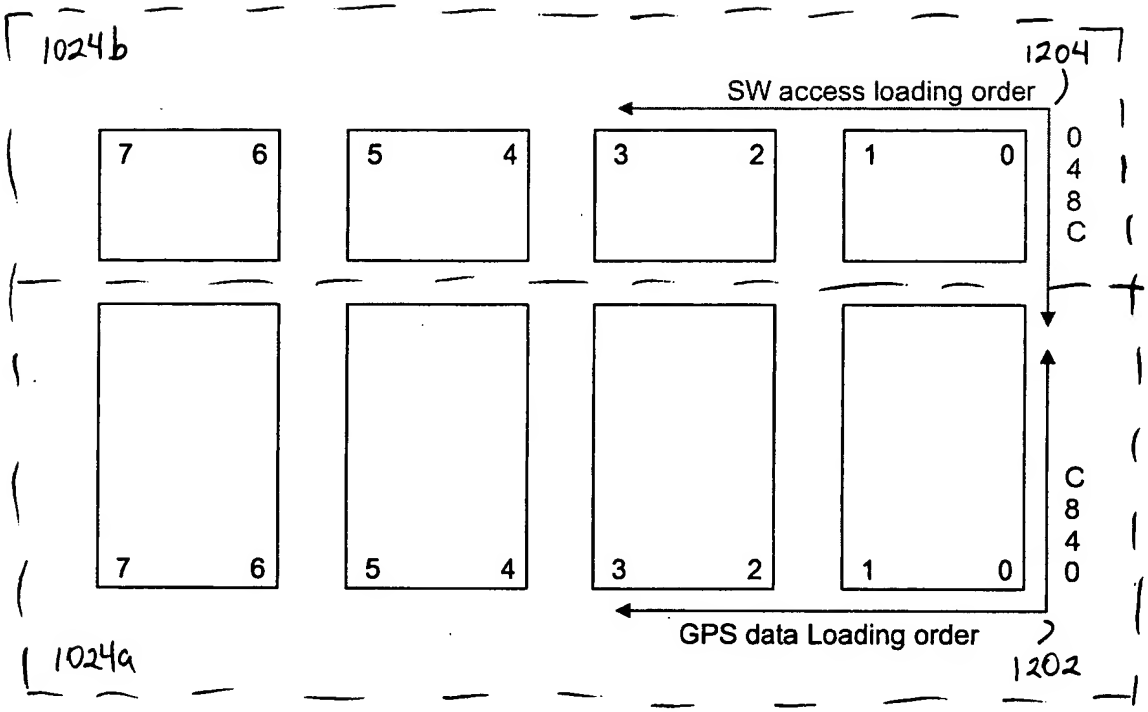
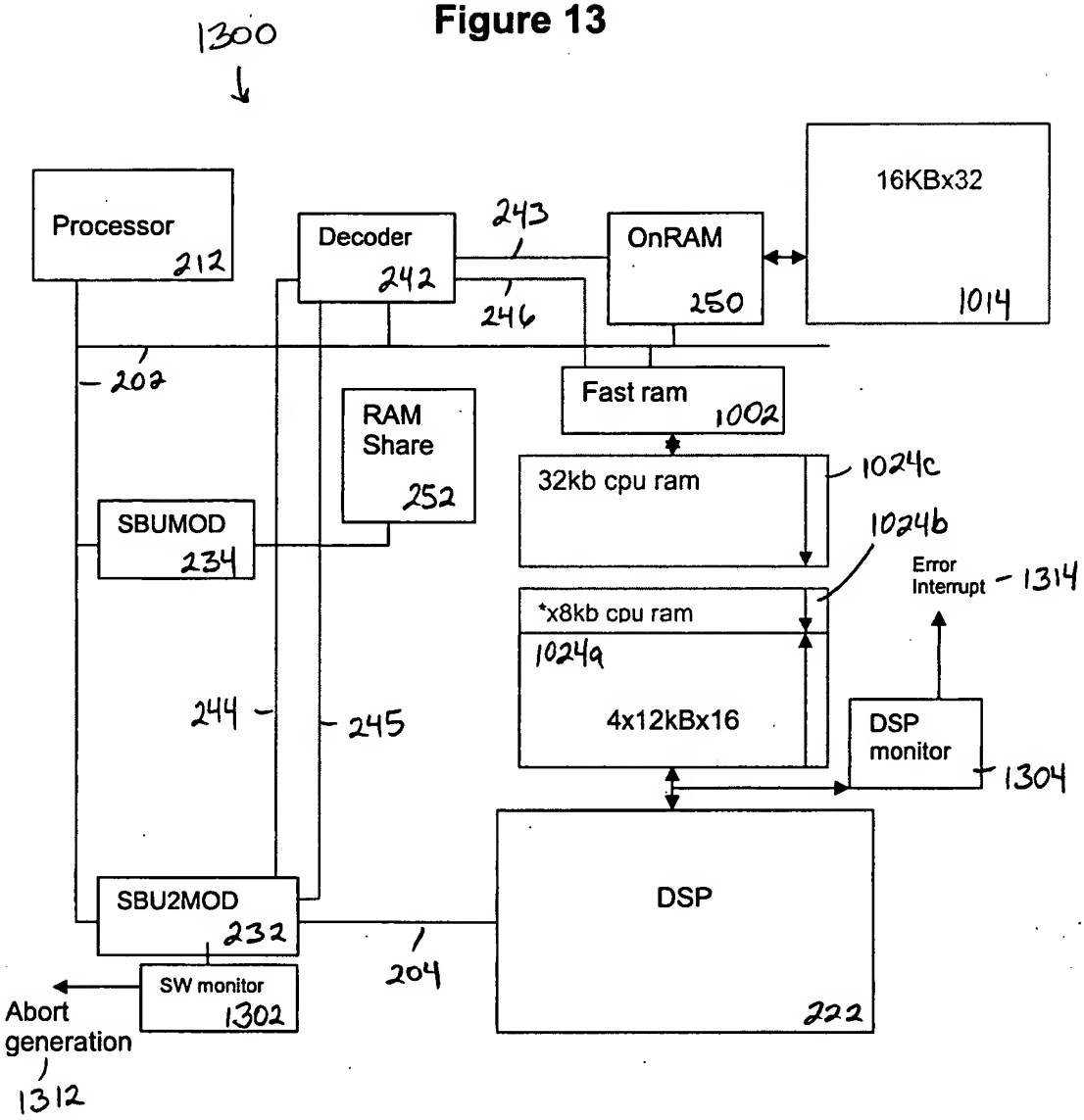

1024b
1204
SW access loading order
7 6
5 4
3 2
1 0
0 4 8 C
C 8 4 0
7 6
5 4
3 2
1 0
GPS data Loading order
1024a
1202

Figure 13


1300
Processor
212
Decoder
242
243
246
OnRAM
250
16KBx32
1014
207
RAM
Share
252
Fast ram
1002
32kb cpu ram
1024c
SBUMOD
234
1024b
Error
Interrupt
1314
*x8kb cpu ram
1024a
4x12kBx16
244
245
DSP
monitor
1304
SBU2MOD
232
DSP
204
SW monitor
1302
222
Abort
generation
1312

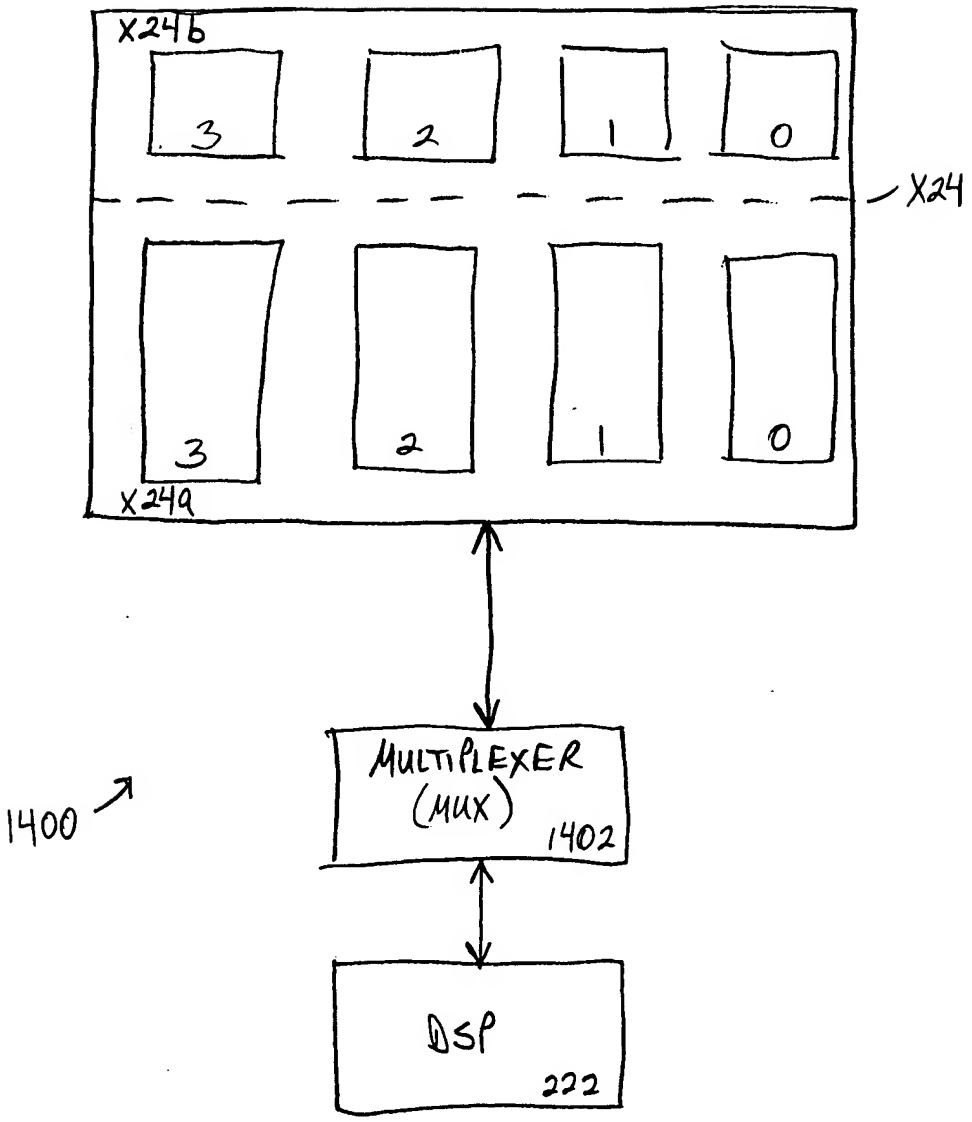


FIGURE 14

RAM_CTL: (address = 0xC0000000)

1500

	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	RW
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-		-	

	7	6	5	4	3	2	1	0
	RW	RW	RW	RW	RW	RW	RW	RW
Reset value	0	0	0	0	0	0	0	0
		SWI_ENB	MAP_BLK[2]	MAP_BLK[1]	MAP_BLK[0]	DSP64K_ MAP_ENB	EN_CPU_WAB	EN_CPU_RAB

Figure 15

RAM_STA: (address = 0xC0000004)

1600

	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-

	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	RW	RW
Reset value	0	0	0	0	0	0	0	0
	-	-	-	-	-	-	CPUW_VIO	CPUR_VIO

Figure 16

DSP_ADDR: (address = 0xC0000008)

1700

	15	14	13	12	11	10	9	8
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
	DSP_ADD [15]	•	•	•	•	•	•	•

	7	6	5	4	3	2	1	0
	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0
	•	•	•	•	•	•	•	DSP_ADD [0]

Figure 17

Figure 18A

1800

Number of 8Kbyte Blocks Mapped	DSP32K_SWI_ENB	DSP64K_MAP_ENB	MAP_BLK[2:0]	DSP Address Range	CPU Normal Mapped SBU2 Address Range	CPU Soft Mapped SBU2 Address Range	CPU Hard Switch ASB Address Range
1	0	0	XXX	0x0000_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	0	1	000	0x0000_0000–0x0001_DFFF	0xC021_E000–0xC021_FFFF	0x6001_0000–0x6001_1FFF	NA
2	0	0	XXX	0x0000_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	0	1	001	0x0000_0000–0x0001_BFFF	0xC021_C000–0xC021_FFFF	0x6001_0000–0x6001_3FFF	NA
3	0	0	XXX	0x0000_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	0	1	010	0x0000_0000–0x0001_9FFF	0xC021_A000–0xC021_FFFF	0x6001_0000–0x6001_5FFF	NA
4	0	0	XXX	0x0001_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	X	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	0	1	011	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	0x6001_0000–0x6001_7FFF	NA
5	0	0	XXX	0x0001_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	1	1	100	0x0000_0000–0x0001_5FFF	0xC021_6000–0xC021_FFFF	0x6001_8000–0x6001_9FFF	0x6001_6000–0x6001_7FFF
	0	1	100	0x0000_0000–0x0001_5FFF	0xC021_6000–0xC021_FFFF	0x6001_0000–0x6001_9FFF	NA
6	0	0	XXX	0x0001_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000–0x0001_7FFF	0xC021_8000–0xC021_FFFF	NA	0x6001_0000–0x6001_7FFF
	1	1	101	0x0000_0000–0x0001_3FFF	0xC021_4000–0xC021_FFFF	0x6001_8000–0x6001_BFFF	0x6001_0000–0x6001_7FFF
	0	1	101	0x0000_0000–0x0001_3FFF	0xC021_4000–0xC021_FFFF	0x6001_0000–0x6001_BFFF	NA
7	0	0	XXX	0x0001_0000–0x0001_FFFF	0xC020_0000–0xC021_FFFF	NA	NA

Number of 8Kbyte Blocks Mapped	DSP32K_SWI_ENB	DSP64K_MAP_ENB	MAP_BLK[2:0]	DSP Address Range	CPU Normal Mapped SBU2 Address Range	CPU Soft Mapped SBU2 Address Range	CPU Hard Switch ASB Address Range
	1	0	XXX	0x0000_0000– 0x0001_7FFF	0xC021_8000– 0xC021_FFFF	NA	0x6001_0000– 0x6001_7FFF
	1	1	110	0x0000_0000– 0x0001_1FFF	0xC021_2000– 0xC021_FFFF	0x6001_8000– 0x6001_DFFF	0x6001_0000– 0x6001_7FFF
	0	1	110	0x0000_0000– 0x0001_1FFF	0xC021_2000– 0xC021_FFFF	0x6001_0000– 0x6001_DFFF	NA
8	0	0	XXX	0x0001_0000– 0x0001_FFFF	0xC020_0000– 0xC021_FFFF	NA	NA
	1	0	XXX	0x0000_0000– 0x0001_7FFF	0xC021_8000– 0xC021_FFFF	NA	0x6001_0000– 0x6001_7FFF
	1	1	111	0x0000_0000– 0x0000_FFFF	0xC021_0000– 0xC021_FFFF	0x6001_8000– 0x6001_EFFF	0x6001_0000– 0x6001_7FFF
	0	1	111	0x0000_0000– 0x0000_FFFF	0xC021_0000– 0xC021_FFFF	0x6001_0000– 0x6001_FFFF	NA

Figure 18B

1800